a protective film over said third metal layer and entirety of said electrode layer, said protective film leaving exposed a central portion of said third metal layer; said electrode layer being capable of passing an emitted light;

said electrode pad being capable of supplying a current to said electrode layer; and

wherein said second metal layer is made of gold (Au), said first metal layer comprises a material that has an ionization potential lower than gold (Au), and said third metal layer comprises aluminum (Al) that has an adhesiveness to said protection film which is stronger than gold (Au) and etching an inner side of said protective film is prevented when a portion of said protective film corresponding to said central portion is etched and said protective film is left on an upper surface of said third metal layer except for said central portion.

12. (Three Times Amended) A light-emitting semiconductor device having a Group III nitride compound semiconductor comprising:

a surface layer made of p-type semiconductor;

a multi-layered electrode layer comprising a first electrode layer formed on said surface layer and a second electrode layer formed on said first electrode layer;

an electrode pad covering a portion of said second electrode layer and leaving another portion of said second electrode layer uncovered; and

wherein said first electrode layer comprises a material which has an ionization potential lower than that of said second electrode layer, said second electrode layer comprises a material which has an ohmic characteristic to said semiconductor better than that of said first electrode layer, and the portion of said material of said second electrode layer which is uncovered by said electrode pad is distributed more deeply into said surface layer than that of said first electrode layer by heat treatment in atmosphere comprising oxygen and provides a

contact resistance between said electrode layer and said surface layer lower than said portion covered with said electrode pad, and a high contact resistance area is formed between said first electrode layer and said surface layer of said p-type semiconductor right under said pad, electric current in downward direction is blocked at said high contact resistance area and flows to a lateral direction.

See the attached Appendix for the changes made to the above claims